

CLAIMS

1. A semiconductor structure comprising:
a first semiconductor region characterized by a dopant concentration
greater than $1 \times 10^{19}/\text{cm}^3$;
5 a second semiconductor region overlying the first semiconductor
region, said second semiconductor region comprising silicon and characterized by a
dopant concentration less than $1 \times 10^{19}/\text{cm}^3$ and a thickness t_1 ; and
a layer comprising titanium directly overlying the second semiconductor
region, said layer characterized by a line width no greater than $0.3\mu\text{m}$ and a
thickness t_2 , wherein $t_1 > 1.2t_2$;
10 t_1/t_2 being sufficiently small that, when the layer is reacted with the
second semiconductor region to form titanium disilicide, the titanium disilicide is in
ohmic contact with the first semiconductor region;
15 t_1/t_2 being sufficiently large that, when the layer is reacted with the
second semiconductor region to form titanium disilicide, the titanium disilicide
anneals to a phase with a sheet resistance less than 3 ohms/square.

Sub A 2. The invention of Claim 1 wherein $t_1 \geq 2.2t_2$.
3. The invention of Claim 1 wherein $t_1 = 2.3t_2, \pm 0.1t_2$.
4. The invention of Claim 1 wherein t_1 is about 600\AA and t_2 is about
20 250\AA .
5. The invention of Claim 1 wherein the dopant concentration of the first
semiconductor region is greater than $1 \times 10^{20}/\text{cm}^3$.
6. The invention of Claim 1 or 5 wherein the first semiconductor region is
doped primarily with boron.

25 A semiconductor structure comprising:
a first semiconductor region characterized by a boron dopant
concentration greater than $1 \times 10^{20}/\text{cm}^3$; and

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a set of titanium silicide conductors directly overlying the first semiconductor region and in ohmic contact therewith, each said conductor characterized by a width no greater than $0.3\mu\text{m}$, and at least 90% of said conductors characterized by a sheet resistance less than 3 ohms/square.

5 8. The invention of Claim 1 or 7 wherein the semiconductor structure comprises a 3-D memory array.

9. A method for forming a semiconductor structure, said method comprising:

(a) forming a first semiconductor region characterized by a dopant concentration greater than $1\times 10^{19}/\text{cm}^3$;

(b) forming a second semiconductor region overlying the first semiconductor region, said second semiconductor region comprising silicon and characterized by a dopant concentration less than $1\times 10^{19}/\text{cm}^3$ and a thickness t_1 ;

(c) forming a layer comprising titanium directly overlying the second semiconductor region, said layer characterized by a line width no greater than $0.3\mu\text{m}$ and a thickness t_2 , wherein $t_1 > 1.2t_2$.

10 15 20 25 10. The method of Claim 9 further comprising:

(d) annealing the second semiconductor region and the layer at a temperature of at least 550°C after (c), thereby forming TiSi_x from the titanium of the layer and the silicon of the second semiconductor region.

11. The method of Claim 10 further comprising:

(e) re-annealing the second conductor region and the layer after (d) at a temperature of at least 750°C , thereby converting the TiSi_x to C54 phase in ohmic contact with the first semiconductor region.

12. The method of Claim 9 wherein the first semiconductor region is formed in (a) with a dopant concentration greater than $1\times 10^{20}/\text{cm}^3$.

13. The method of Claim 9 or 12 wherein the first semiconductor region formed in (a) is doped primarily with boron.

14. A method for forming a semiconductor structure, said method comprising:

(a) forming a heavily doped first semiconductor region;
(b) forming a second semiconductor region comprising silicon and
5 overlying the first semiconductor region, said second semiconductor region less
heavily doped than said first semiconductor region and characterized by a thickness
 t_1 ;

(c) forming a layer comprising titanium directly overlying the second
semiconductor region, said layer characterized by a line width no greater than $0.3\mu\text{m}$
10 and a thickness t_2 , wherein $t_1 > 1.2t_2$; and

(d) annealing the second conductor region and the layer after (c) at
a temperature of at least 750°C , thereby forming a low-resistivity, C54-phase TiS_2
film in ohmic contact with the first semiconductor region.

15. The method of Claim 9 or 14 wherein the semiconductor structure
comprises a 3-D memory array.

16. The method of Claim 9 or 14 wherein $t_1 \geq 2.2t_2$.

17. The method of Claim 9 or 14 wherein $t_1 = 2.3t_2 \pm 0.1 t_2$.